

AMENDMENTS TO THE CLAIMS

Claims 1-6. (Canceled)

7. (Currently Amended) A method of forming a varactor diode in a substrate, comprising:
- forming a well region of a first conductivity type in the substrate;
 - forming a plurality of isolation regions on upper portions of the well region;
 - forming a plurality of masking structures having first and second sides formed on the substrate between respective ones of said plurality of isolation regions;
 - forming a first plurality of diffusion regions of a second conductivity type, at least some of said first plurality of diffusion regions abutting respective ones of said plurality of isolation regions and at least a first of said first plurality of diffusion regions that does not abut respective ones of said plurality of isolation regions; and
 - forming a second plurality of diffusion regions of said first conductivity type, a first of said second plurality of diffusion regions abutting portions of said at least first of ~~said first plurality of diffusion regions that do not abut respective ones of said plurality of isolation regions,~~ said second plurality of diffusion regions extending below respective sides of respective ones of said plurality of masking structures, wherein respective ones of said second plurality of diffusion regions do not contact one another.
8. (Original) The method of claim 7, further comprising forming a first electrical connection that interconnects said first plurality of diffusion regions.
9. (Original) The method of claim 8, further comprising forming a second electrical connection to said well region.
10. (Currently Amended) The method of claim 7, wherein said step of forming said ~~second~~ first plurality of diffusion regions comprises an angled implant.

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11. (Currently Amended) The method of claim 10, wherein said angled implant is carried out at an angle of approximately between approximately 7 and 60 degrees with respect to a plane of the substrate.

Claims 12-14. (Canceled)

15. (Currently Amended) A method of forming an integrated circuit on a semiconductor substrate, comprising:
- forming first and second well regions of a first conductivity type in the substrate;
 - forming a plurality of isolation regions on upper portions of each of said well regions;
 - forming a plurality of conductive structures having first and second sides on each of said first and second well regions, said plurality of conductive structures comprising a plurality of masking structures on said first well regions and gate electrodes on said second well regions;
 - masking said second well regions;
 - forming a first plurality of diffusion regions of a second conductivity type in said first well regions, at least some of said plurality of diffusion regions abutting respective ones of said plurality of isolation regions and at least a first of said first plurality of diffusion regions that does not abut respective ones of said plurality of isolation regions;
 - and
 - forming a second plurality of diffusion regions of said first conductivity type in said first well regions, a first of said second plurality of diffusion regions abutting portions of said at least first of said first plurality of diffusion regions ~~that do not abut respective ones of said plurality of isolation regions~~, said second plurality of diffusion regions extending below respective sides of respective ones of said plurality of masking

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structures, wherein respective ones of said second plurality of diffusion regions do not contact one another.

16. (Original) The method of claim 15, wherein said substrate is selected from the group consisting of silicon, SiGe, and Group III-V semiconductors.
17. (Original) The method of claim 16, wherein said substrate is doped with an atom that increases strain and hence mobility of minority carriers.

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